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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,001	10/21/2003	Martin Brox	S&ZIO031002	4857
24131	7590	08/04/2005	EXAMINER	
LERNER AND GREENBERG, PA P O BOX 2480 HOLLYWOOD, FL 33022-2480			CHO, JAMES HYONCHOL	
			ART UNIT	PAPER NUMBER
			2819	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/690,001

Applicant(s)

BROX, MARTIN

Examiner

James Cho

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 7-19-2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 6-8 is/are rejected.
- 7) ☒ Claim(s) 5 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

Receipt is acknowledged of the Amendment filed 7-19-2005.

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 are rejected under 35 U.S.C. 102(b) as being anticipated by Suh (US PAT No. 6,140,841).

Regarding claims 1 and 8, Figs. 2 and 6A of Suh teaches a driver stage (Fig. 6A) for driving an output on one of n levels (4 levels, Fig. 7) or a method of manufacturing a driver stage, which are each spaced from each other by a voltage difference of dV (see TABLE 6 on col. 6), comprising: a plurality of field effect transistors (MP61, 62 and MN61, 62) for driving the output by leading a current to or away from the output (see the drive current in TABLE 6), with the relationship of the channel widths of at least two field effect transistors, which both act either for leading current to or away from, being set in dependence on the value of the voltage difference (different data signals creates different channel width, which translates into different voltages, channel width and voltage are dependent each other, i.e. an output level of the driver in Fig. 6A provided to the receiver circuit in Fig. 6B is based on a corresponding channel width as well as a different channel width selected by Datax and Datay produces a corresponding output level).

Regarding claim 2, Figs. 2 and 6A of Suh teaches the driver stage in accordance with claim 1, further comprising: a terminal circuit ( $R_{tt}$  and  $V_{tt}$  in Fig. 2) connected to the output and comprising means for applying a terminal voltage ( $V_{tt}$ ) and a terminal resistor ( $R_{tt}$ ) connected in series between the means for applying a terminal voltage and an output ( $R_{tt}$  is in series with  $V_{tt}$  and the output DQ).

Regarding claim 3, Figs. 2 and 6A of Suh teaches the driver stage in accordance with claim 1, with the plurality of field effect transistors comprising: a first and a second field effect transistor (MP61, 62) connected in parallel to each other voltage, and a third and a fourth field effect transistor (MN61, 62) being connected in parallel to each other between the output and ground.

Regarding claim 4, Figs. 2 and 6A of Suh teaches the driver stage in accordance with claim 1, further comprising a control means (61) for turning the field effect transistors on and off, depending on a plurality of input bit signals (Datax, Datay, en) in accordance with an allocation rule, which associates a selection of field effect transistors to be turned on and off with each bit combination of bit values of the input bit signals (see TABLE 6).

Regarding claim 6, Figs. 2 and 6A of Suh teaches the driver stage in accordance with claim 1 wherein the at least two field effect transistors are operated in the linear

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range (equal ratio of driving current  $I_o$  to the channel width requires inherently required the transistors being operated in linear range).

Regarding claim 7, Figs. 2 and 6A of Suh teaches the driver stage in accordance with claim 1, wherein the relationship is greater than 2 (TABLE 3 shows the ratio being 3, e.g.  $3W_N/1W_N = 3$ ).

### ***Response to Arguments***

Applicant's arguments filed 7-19-2005 have been fully considered but they are not persuasive.

The applicant argues that SUH reference (US PAT No. 6,140,841) does not anticipate the features of claims 1 and 8. On page 9 of the amendment, the applicant argues that "SUH discloses that the ratios of the channel width of the field-effect transistors of a driver stage are set independently of the value of the voltage difference between the n-output levels". The examiner notes the different channel widths are set as shown on Table 6 on col. 6 of SUH so that the output level of the driver in Fig. 6A provided to the receiver circuit in Fig. 6B is based on a corresponding channel width as well as a different channel width selected by Datax and Datay produces a corresponding output level. Therefore, there is a dependent relationship between the channel widths of at least two field effect transistors and the output voltage of the driver. The examiner further notes that the statement, "the ratios of the channel width of the field-effect transistors", is not found in claim languages. The applicant further argues that the dependence between the channel width and voltage is a general relationship for

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individual channel width settings and not directed to a relationship between two different channel widths. The examiner notes that SUH reference teaches all the broadly claimed limitations of the instant application; "the relationship of the channel widths of at least two field effect transistors..., being set in dependence on the value of the voltage difference" where four transistors having its own channel widths determines the output voltage of the driver as well as the output voltage of the driver is determined (i.e. depended) by the channel widths being selected by the Datax and Datay as discussed in col. 5, line 28 - col. 6, line 47 of the specification.

***Allowable Subject Matter***

Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802.

The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



James Cho

Primary Examiner

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Date: 4-15-2005